7th International Symposium on Networks-on-Chip (NOCS’13)  
April 21st – 24th, 2013, Tempe, AZ.

Program

Sunday, April 21, 2013 – Tutorial Day

Tutorial Location: BYENG 210, 699 S. Mill Ave., Tempe, AZ, 85281 (5 mins walk from NOCS site)

8.45--12.00 Tutorial 1
MILLIMETER (mm)-WAVE WIRELESS NoC AS INTERCONNECTION BACKBONE FOR MULTICORE CHIPS: PROMISES AND CHALLENGES
Partha Pratim Pande, Washington State University, Pullman, WA; Manos M. Tentzeris, Georgia Institute of Technology, Atlanta, GA; Deukhyoun Heo, Washington State University, Pullman, WA.

12.00--1.30 Lunch

1.30--4.45 Tutorial 2
AUTOMATIC DEADLOCK VERIFICATION IN WORMHOLE NETWORK-ON-CHIPS
Julien Schmaltz and Freek Verbeek
Open University of the Netherlands, Heerlen, The Netherlands.

6.30-8.30 Welcome reception (Courtyard West, Tempe Mission Palms Hotel)

Monday April 22, 2013 – NOCS Day 1

8.15--8.30 Welcome Address

8:30--9:30 Keynote Address
HETEROGENEOUS INTERCONNECTS FOR HETEROGENEOUS COMPUTING
Luca Benini
University of Bologna, Bologna, Italy.

9:30--9:45 Coffee Break

9.45--11:05 Session 1
Emerging Technology: Optics, Wireless and 3D
Session Chair: Ajay Joshi, Boston University.

1.1 ENERGY-EFFICIENT ADAPTIVE WIRELESS NOCS ARCHITECTURE
Dominic DiTomaso, Avinash Kodi, David Matolak, Savas Kaya, Soumyasanta Laha and William Rayess
1.2 PROBE: PREDICTION-BASED OPTICAL BANDWIDTH SCALING FOR ENERGY-EFFICIENT NOCS
   Li Zhou and Avinash Kodi

1.3 LUMINOC: A POWER-EFFICIENT, HIGH-PERFORMANCE, PHOTONIC NETWORK-ON-CHIP FOR FUTURE PARALLEL ARCHITECTURES (S)
   Mark Browning, Cheng Li, Paul Gratz and Samuel Palermo

1.4 3D LOGARITHMIC INTERCONNECT: STACKING MULTIPLE L1 MEMORY DIES OVER MULTI-CORE CLUSTERS (S)
   Erfan Azarkhish, Igor Loi and Luca Benini

1.5 LEVERAGING THE GEOMETRIC PROPERTIES OF ON-CHIP TRANSMISSION LINE STRUCTURES TO IMPROVE INTERCONNECT PERFORMANCE: A CASE STUDY IN 65NM (S)
   Shomit Das, Georgios Manetas, Kenneth Stevens and Roberto Suaya

11:05--12:00 Poster Session I + Coffee Break

12:00--1:30 Lunch
   Café Boa, 398 S Mill Ave, Tempe, AZ 85281. (We will walk from the meeting room)

1:30--3.05 Session 2
Routing Algorithms
Session Chair: Danella Zhao, University of Louisiana at Lafayette

2.1 GCA: GLOBAL CONGESTION AWARENESS FOR LOAD BALANCE IN NETWORKS-ON-CHIP
   Mukund Ramakrishna, Paul Gratz and Alexander Sprintson

2.2 HEADFIRST SLIDING ROUTING: A TIME-BASED ROUTING SCHEME FOR BUS-NOC HYBRID 3-D ARCHITECTURE
   Takahiro Kagami, Hiroki Matsutani, Michihiro Koibuchi and Hideharu Amano

2.3 A GREEDY APPROACH FOR LATENCY-BOUNDED DEADLOCK-FREE ROUTING PATH ALLOCATION FOR APPLICATION-SPECIFIC NOCS
   Amit Verma, Pritpal Singh Multani, Daniel Mueller-Gritschneder, Vladimir Todorov and Ulf Schlichtmann

2.4 A DEADLOCK-FREE ROUTING ALGORITHM REQUIRING NO VIRTUAL CHANNEL ON 3D-NOCS WITH PARTIAL VERTICAL CONNECTIONS (S)
   Jinho Lee and Kiyoungh Choi

2.5 SNET, A FLEXIBLE, SCALABLE NETWORK PARADIGM FOR MANYCORE ARCHITECTURES (S)
   Celine Azar, Stephane Chevobbe, Yves Lhuiller and Jean-Philippe Diguet

3:05--4:00 Poster Session 2 + Coffee Break
4:00–5:00 Session 3
Fault Tolerance and Reliability
Session Chair: Zhonghai Lu, KTH

3.1 AN NOC AND CACHE HIERARCHY SUBSTRATE TO ADDRESS EFFECTIVE VIRTUALIZATION AND
FAULT-TOLERANCE
Mario Lodde and José Flich

3.2 MINIMAL-PATH FAULT-TOLERANT APPROACH USING CONNECTION-RETAINING STRUCTURE
IN NETWORKS-ON-CHIP
Masoumeh Ebrahimi, Masoud Daneshtalab, Juha Plosila and Hannu Tenhunen

3.3 BACKWARD PROBING DEADLOCK DETECTION FOR NETWORKS-ON-CHIP (S)
Yean-Ru Chen, Zi-Rong Wang, Pao-Ann Hsiung, Sao-Jie Chen and Meng-Hsun Tsai

5.00-5:45 Poster Session 3 + Coffee Break

Tuesday April 23, 2013 – NOCS Day 2

8.30-9.30 Keynote Address
UNDERSTANDING NETWORKS-ON-CHIP: A DECADE AND BEYOND
Radu Marculescu
Carnegie Mellon University, Pittsburgh, PA.

9.30-9:45 Coffee Break

9.45-11:10 Session 4
Simulation and Modeling
Session Chair: Sudeep Pasricha, Colorado State University.

4.1 SCALABLE PARALLEL SIMULATION OF NETWORKS ON CHIP
Marcus Eggenberger and Martin Radetzki

4.2 PER-FLOW DELAY BOUND ANALYSIS BASED ON A FORMALIZED MICROARCHITECTURAL
MODEL
Xueqian Zhao and Zhonghai Lu

4.3 AN ACCURATE AND SCALABLE ANALYTIC MODEL FOR ROUND-ROBIN ARBITRATION IN
NETWORK-ON-CHIP
Erik Fischer and Gerhard P. Fettweis

4.4 PHYSICAL PLANNING FOR THE ARCHITECTURAL EXPLORATION OF LARGE-SCALE CHIP
MULTIPROCESSORS (S)
Javier De San Pedro, Nikita Nikitin, Jordi Cortadella and Jordi Petit
11.10--12.00 Poster Session 4

12:00--1:30 Lunch
Courtyard West, Tempe Mission Palms (Symposium site)

1:30--2:30 Session 5
Potpourri
Session Chair: Serag Gadelrab, Qualcomm

5.1 ACCELERATING ATOMIC OPERATIONS ON THE GPU FOR BROADER APPLICABILITY
Sean Franey and Mikko Lipasti

5.2 A SPECULATIVE ARBITER DESIGN TO ENABLE HIGH-FREQUENCY MANY-VC ROUTER IN NOCS
Bo Zhao, Youtao Zhang and Jun Yang

5.3 QUADRISECTION-BASED TASK MAPPING ON MANY-CORE PROCESSORS FOR ENERGY-EFFICIENT ON-CHIP COMMUNICATION (S)
Nithin Michael, Yao Wang, Kevin Tang and Edward Suh

2:30--3:15 Poster Session 5 + Coffee Break

3:15--5:15 Special Session on Emerging Interconnects Technologies
Organizers: Ahmed Louri, University of Arizona, and Avinash Kodi, Ohio University.
Panelists: Vijaykrishnan Narayanan, Pennsylvania State University; Kannan Raj, Oracle Labs; Sudhakar Yalamanchili, Georgia Tech; Partha Pande, Washington State University.

6.30--10.00 Banquet
Tempe Mission Palms (Symposium site)

Wednesday April 24, 2013 – NOCS Day 3

8.30--9:30 Keynote Address
COMMUNICATION CHALLENGES IN ACCELERATOR-RICH ARCHITECTURES
Ravishankar Iyer,
Intel Corporation, Hillsboro, OR.

9:30--9:45 Coffee Break

9:45--11:00 Session 6
Network Architecture
Session Chair: Bin Li, Intel

6.1 DYNAMIC TRAFFIC DISTRIBUTION AMONG HIERARCHY LEVELS IN HIERARCHICAL NETWORKS-ON-CHIP (NOCS)
Ran Manevich, Israel Cidon and Avinoam Kolodny
6.2 CENTRALIZED BUFFER ROUTER: A LOW LATENCY, LOW POWER ROUTER FOR HIGH RADIX NOCS
Syed Minhaj Hassan and Sudhakar Yalamanchili

6.3 ON SELF-TUNING NETWORKS-ON-CHIP FOR DYNAMIC NETWORK-FLOW DOMINANCE ADAPTATION
Xiaohang Wang, Terrence Mak, Mei Yang, Yingtao Jiang, Masoud Daneshtalab and Maurizio Palesi

11:00–12.00 Poster Session 6 + Coffee Break

12.00–12.30 Closing session
   Best Paper Award Announcement

12.30–2.00 Lunch
   Mellow Mushroom, 750 S. Mill Avenue, Suite #D100, Tempe, AZ 85281 (We will walk from the meeting room)
Wireless connectivity and web downloads

Hotel wireless
Network id: tmph or ephostream
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NOCS’13 tutorials proceedings
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Maps for conference events

Directions for Sunday tutorial
BYENG 210, 699 South Mill Avenue

Tutorial site is in room BYENG 210 on ASU campus. BYENG is the big red brickyard building on Mill Avenue at 699 South Mill Avenue. From the Plaza level at Brickyard please take either the escalator, stairs or the elevator to the 2\textsuperscript{nd} floor for BYENG 210.

Directions for Monday lunch
Café Boa, 398 South Mill Avenue

Directions for Wednesday lunch
Mellow Mushroom, 750 South Mill Avenue