CURRICULUM VITAE

KARAMVIR S. CHATHA

ASSOCIATE PROFESSOR,
DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING,
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1 Background

a. Education

- **PhD in Computer Science and Engineering**,
  University of Cincinnati, Cincinnati, OH, 2001.
  Dissertation System-level Co-synthesis of Transformative Applications for Heterogeneous Hardware-Software Architectures

- **MS in Computer Science and Engineering**,
  University of Cincinnati, Cincinnati, OH, 1997.
  Thesis Performance Evaluation Tool for Non-pipelined and Pipelined Hardware-Software Codesigns

- **BE in Computer Technology**,
  University of Mumbai, Mumbai, India, 1993.

b. Academic Experience

- 8/08-now **Associate Professor**
  Department of Computer Science and Engineering, Arizona State University.

- 8/01-7/08 **Assistant Professor**
  Department of Computer Science and Engineering, Arizona State University.

- 6/95-8/01 **Research Assistant**
  Department of Electrical & Computer Engineering,and Computer Science, University of Cincinnati.

- 8/94-5/95 **Teaching Assistant**
  Department of Electrical & Computer Engineering,and Computer Science, University of Cincinnati.

c. Principal Areas of Teaching and Research

- **Teaching** Digital hardware design and synthesis
  VLSI design automation
  System-level hardware-software co-design

- **Research** Computer-aided design of VLSI and embedded systems
  Network-on-Chip design and optimization
  Multi-processor System-on-Chip design
  Low power and thermal aware design
  Hardware-software co-design
  Reconfigurable and adaptive computing

d. Awards and Honors

- **National Science Foundation CAREER Award** for "System-level Design of Network-on-Chip Architectures", 2006.
- **IEEE/ACM William J. McCalla ICCAD Best Paper Award** for "Approximation Algorithm for the Temperature Aware Scheduling Problem" at International Conference Computer-Aided Design (ICCAD), 2007, San Jose, CA.
- **Best Paper Award** for "Hardware-Software Co-design for Dynamically Re-configurable Architectures" at Field Programmable Logic and Applications Workshop (FPL), 1999, Glasgow, Scotland.
- **Travel Award** to attend NATO Advanced Study Institute Workshop on *"System-level Synthesis,"* Italy, August, 1998.
- **University Graduate Scholarship**, University of Cincinnati, *Fall 1993-1999*.

2 Publications

In the following list of papers, student co-authors are denoted in **boldface**. In case of joint publications with other faculty, the faculty making the major contribution is identified with an asterisk.

a. Refereed Archival Journal Papers

1. "Approximation Algorithms for Design of Application Specific Network-on-Chip Architectures"
   Karam S. Chatha*, **Krishnan Srinivasan** and Goran Konjevod,
   accepted for *IEEE Transactions on Computer-aided Design of Integrated Circuits*.

2. "Design of Network-on-Chip Architectures with Genetic Algorithm based Technique",
   Glenn Leary, Karam S. Chatha, **Krishna Mehta** and **Krishnan Srinivasan**
   accepted for *IEEE Transactions on VLSI Systems*.

3. "Integer Linear Programming and Heuristic Techniques for System-level Design on Multi-core and Block Multi-threaded Network Processor Architectures",
   Chris Ostler, **Vijay Ramamurthi**, Karam S. Chatha and **Krishnan Srinivasan**,
   ACM Transactions on Design Automation for Electronic Systems, Vol. 12, No. 4, Article 48, pp 48:1-48:40, 2007.

4. "Integer Linear Programming and Heuristic Techniques for System-level Low Power Scheduling on Multiprocessor Architectures under Throughput Constraints",
   Krishnan Srinivasan and Karam S. Chatha,
   Integration, VLSI Journal, Elsevier publications, Vol. 40, Issue 3, pp 326-354, 2007.

5. "Optimization of Media Processing Workflows with Adaptive Operator Behaviors",
   Lina Peng, K.Selcuk Candan*, **Chris Mayer**, Kyung D. Ryu, and Karam S. Chatha,
   Multimedia Tools and Applications Journal, Kluwer Academic Publishers, Volume 33, Number 3, 2007.

6. "Linear Programming based Techniques for Synthesis of Application Specific Network-on-Chip Architectures",
   Krishnan Srinivasan, Karam S. Chatha* and Goran Konjevod,
   IEEE Transactions on VLSI Systems, Vol 14, No. 4, pp 407-420, 2006.

7. "Quality-of-Service and Error Control Techniques for Mesh based Network-on-Chip Architectures",
   Praveen Vellanki, **Nilanjan Banerjee**, and Karam S. Chatha,
   Integration, VLSI Journal, Elsevier Publications, Vol. 38, Issue 3, pp 353-382, 2005.

8. "Hardware-Software Partitioning and Pipelined Scheduling of Transformative Applications",
   Karam S. Chatha and Ranga Vemuri,
   IEEE Transactions on VLSI Systems, Vol. 10, Issue 3, pp 193-208, 2002.

9. "An Iterative Algorithm for Partitioning, Hardware Design Space Exploration and Scheduling of Hardware-Software Systems",
   Karam S. Chatha and Ranga Vemuri,
   Design Automation for Embedded Systems Journal, Kluwer Academic Publishers, No. 5, pp 281-293, August, 2000.

Refereed Archival Journal Papers Under Review

10. "Approximation Algorithms for Temperature Aware and Low Power Scheduling Problems"
    Sushu Zhang and Karam S. Chatha,
    submitted to *ACM Transactions on Design Automation for Electronic Systems*, under review.

11. "An Automated Heuristic Technique for Design of Custom Network-on-Chip Architectures",
    Krishnan Srinivasan and Karam S. Chatha,
    submitted to *ACM Transactions on Design Automation for Electronic Systems*, under revision after first review.

12. “A Technique for Energy versus Quality-of-Service Trade-off for MPEG-2 Decoder”,
Krishnan Srinivasan and Karam S. Chatha,
submitted to *IEEE Transactions on VLSI Systems*, under revision after first review.

b. National and International Conference Proceedings Refereed Papers (highly selective forums)

The acceptance rates of the highly selective forums wherever available are also specified. All conference proceeding publications (except for 30 and 34 which had poster presentations, and 32 which was a demonstration) were accompanied by a presentation.

1. ”System-level Thermal Aware Design of Applications with Uncertain Execution Times”,
Sushu Zhang and Karam S. Chatha,
Accepted for *Proceedings of International Conference on Computer-Aided Design (ICCAD)*, November 10-13, San Jose, CA, 2008.

2. ”Power Reduction via Macroblock Prioritization for Power Aware H.264 Video Applications ,
Mike Baker, and Karam S. Chatha,
Accepted for *Proceedings of International Conference on Hardware-Software Codesign and System Synthesis (CODES-ISSS)*, October 19-24, Atlanta,GA 2008.

3. ”Automated Techniques for Energy Efficient Scheduling on Homogeneous and Heterogeneous Chip Multi-processor Architectures ”,
Sushu Zhang and Karam S. Chatha,
Proceedings of Asia South Pacific Design Automation Conference (ASPDAC), January 21-24, Seoul, South Korea, 2008.
Acceptance rate: 123/350, 35%

4. ”Approximation Algorithm for the Temperature Aware Scheduling Problem”,
Sushu Zhang and Karam S. Chatha,
Proceedings of International Conference on Computer-Aided Design (ICCAD), November 10-14, San Jose, CA, 2007.
Acceptance rate: 139/510, 27.3%
Recipient of the IEEE/ACM William J. McCalla ICCAD Best Paper Award (1/139 papers).

5. ”Performance and Resource Optimization of NoC Router Architecture for Master and Slave IP Cores”,
Glenn Leary, **Krishna Mehta** and Karam S. Chatha,
Proceedings of International Conference on Hardware/Software Co-design and System Synthesis (CODES-ISSS), September 30- October 5, Salzburg, Austria, 2007.

6. ”Smart Driver for Power Reduction in Next Generation Bi-Stable Electrophoretic Display Technology”,
Michael Baker, Aviral Shrivastava*, and Karam S. Chatha,
Proceedings of International Conference on Hardware/Software Co-design and System Synthesis (CODES-ISSS), September 30- October 5, Salzburg, Austria, 2007.

7. ”Approximation Algorithms for Power Minimization of Earliest Deadline First and Rate Monotonic Schedules”,
Sushu Zhang, Karam S. Chatha*, and Goran Konjevod
Proceedings of International Symposium on Low Power Electronic Design (ISLPED), August 27-29, Portland, OR, 2007.

8. ”Approximation Algorithm for Data Mapping on Block Multi-threaded Network Processor Architectures”,
Chris Ostler and Karam S. Chatha,
Proceedings of IEEE/ACM Design Automation Conference (DAC), June 4-8, San Diego, CA, 2007.

9. ”An ILP Formulation for System-Level Application Mapping on Network Processor Architectures”,
Chris Ostler and Karam S. Chatha,
Proceedings of IEEE/ACM Design Automation and Test in Europe Conference (DATE), April 16-20, Nice, France, 2007.
Acceptance rate: 208/933, 22.3%

10. ”Approximation Algorithm for Process Mapping on Network Processor Architectures”,
Chris Ostler, Karam S. Chatha*, and Goran Konjevod,
Proceedings of Asia South Pacific Design Automation Conference (ASPDAC), January 23-26, Yokohama, Japan, 2007.
Acceptance rate: 131/408, 32.1%

11. ”Application Specific Network-on-Chip Design with Guaranteed Quality Approximation Algorithms”,
Krishnan Srinivasan, Karam S. Chatha*, and Goran Konjevod,
Proceedings of Asia South Pacific Design Automation Conference (ASPDAC), January 23-26, Yokohama, Japan, 2007.
Acceptance rate: 131/408, 32.1%

12. ”Layout Aware Design of Mesh Based Network-on-Chip Architectures”,
Krishnan Srinivasan, and Karam S. Chatha,
Proceedings of International Conference on Hardware/Software Codesign and System Synthesis (ISSS-CODES), October 22-25, Seoul, Korea, 2006.
Acceptance rate: 46/183, 25%

13. “A Low Complexity Heuristic for Design of Custom Network-on-Chip Architectures”,
Krishnan Srinivasan, and Karam S. Chatha,
Proceedings of IEEE/ACM Design Automation and Test in Europe (DATE), March 6-10, Munich, Germany, 2006.
Acceptance rate: 267/834, 32 %

14. “An Automated Technique for Topology and Route Generation of Application Specific On-Chip Interconnection Networks”,
Krishnan Srinivasan, Karam S. Chatha*, and Goran Konjevod,
Proceedings of IEEE/ACM International Conference on Computer-aided Design (ICCAD), November 6-10, San Jose, CA, 2005.
Acceptance rate : 128/540, 23.7 %

15. “A Technique for Low Energy Mapping and Routing in Network-on-Chip Architectures”,
Krishnan Srinivasan, and Karam S. Chatha,
Proceedings of International Symposium on Low Power Electronic Design, San Diego, CA, August 8-10, 2005.
Acceptance rate : 53/233, 22.7 %

16. “System-level Methodology for Programming CMP based Multi-threaded Network Processor Architectures”,
Vijay Ramamurthi, **Jason McCollum**, **Christopher Ostler**, and Karam S. Chatha,
Proceedings of IEEE Computer Society Annual Symposium on VLSI, Clearwater, FL, May, 2005.
Acceptance rate : 37/126, 29.4%

17. “SAGA: Synthesis Technique for Guaranteed Throughput NoC Architectures”,
Krishnan Srinivasan and Karam S. Chatha,
Proceedings of Asia South-Pacific Design Automation Conference (ASPDAC), Shanghai, China, January 19-21, 2005.
Acceptance rate : 185/692, 26.7 %

18. “ISIS: A Genetic Algorithm based Technique for Custom On-Chip Interconnection Network Synthesis”,
Krishnan Srinivasan and Karam S. Chatha,

Proceedings of 18^{th} *International Conference on VLSI Design (IVLSI)*, Kolkata, India, January 3-7, 2005.
Acceptance rate : 113/352, 32.1%

19. "A Technique for Throughput and Register Optimization During Resource Constrained Pipelined Scheduling",
Nagendran Rangan and Karam S. Chatha,
Proceedings of 18^{th} *International Conference on VLSI Design (IVLSI)*, Kolkata, India, January 3-7, 2005.
Acceptance rate : 113/352, 32.1%

20. "Linear Programming based Techniques for Synthesis of Network-on-Chip Architectures",
Krishnan Srinivasan, Karam S. Chatha* and Goran Konjevod,
Proceedings of International Conference on Computer Design (ICCD), October 11-13, 2004, San Jose, CA.
Acceptance rate : 84/226, 37%

21. "Quality-of-Service and Error Control Techniques for Network-on-Chip Architectures",
Praveen Vellanki, **Nilanjan Banerjee**, and Karam S. Chatha,
Proceedings of the 14^{th} *ACM Great Lakes Symposium on VLSI*, Boston, MA, April 26-28, 2004.
Acceptance rate: 23/237, 9.7%

22. "System-level Design Techniques for Throughput and Power Optimization of Multiprocessor SoC Architectures",
Krishnan Srinivasan, **Nagendar Telkar**, **Vijay Ramamurthi**, and Karam S. Chatha,
Proceedings of IEEE Computer Society Annual Symposium on VLSI, Lafayette, LA, February 19-20, 2004.
Acceptance rate: 29/123, 23%

23. "A Power and Performance Model for Network-on-Chip Architectures",
Nilanjan Banerjee, **Praveen Vellanki**, and Karam S. Chatha,
Proceedings of Design Automation and Test in Europe Conference, Paris, France, February 16-20, 2004.
Acceptance rate : 181/780, 27%

24. "An ILP Formulation for System-level Throughput and Power Optimization in Multiprocessor SoC Architectures",
Krishnan Srinivasan, and Karam S. Chatha,
Proceedings of 17^{th} *International Conference on VLSI Design*, Mumbai, India, January 5-9, 2004.
Acceptance rate : 100/330, 30.3%

25. "MAGELLAN: Multiway Hardware-Software Partitioning and Scheduling for Latency Minimization of Hierarchical Control-Dataflow Task Graphs",
Karam S. Chatha and Ranga Vemuri,
Proceedings of 9th International Symposium on Hardware/Software Codesign, Copenhagen, Denmark, April 25-27, 2001.
Acceptance rate : 23/83, 27.7 %

26. "Hardware Software Codesign for Dynamically Reconfigurable Architectures",
Karam S. Chatha and Ranga Vemuri,
Proceedings of 9th International Workshop on Field Programmable Logic and Applications, Glasgow, Scotland, August 30-September 1, 1999.
Best Paper Award

27. "A Tool for Partitioning and Pipelined Scheduling of Hardware-Software Systems",
Karam S. Chatha and Ranga Vemuri,
Proceedings of 11th International Symposium on System Synthesis, Hsinchu, Taiwan, R.O.C., December 2-4, 1998.
Acceptance rate : 18/63, 28.3 %

28. "RECOD: A Retiming Heuristic to Optimize Resource and Memory Utilization in HW/SW Codesigns",
Karam S. Chatha and Ranga Vemuri,
Proceedings of 6th International Workshop Hardware/Software Codesign, Seattle, Washington, pp 139-145, March 15-18, 1998.
Acceptance rate : 24/66, 36.4 %

Other National and International Conference Proceedings Refereed Papers

29. ”Vulnerabilities of PKI based Smartcards”,
Partha Dasgupta, Karam S. Chatha and Sandeep Gupta,
Proceedings of IEEE Military Communications Conference (MILCOM), October 29-31, Orlando, FL, 2007.

30. ”Modular Design of Media Retrieval Workflows Using ARIA”,
Lina Peng, **Gisik Kwon**, **Y. Chen**, K. Seluk Candan*, Hari Sundaram, Karam S. Chatha, Maria L. Sapino,
Proceedings of 5th International Conference on Image and Video Retrieval (CIVR), July 13-15, Tempe, AZ, 2006.

31. “Layout Aware Design of Custom Network-on-Chip Architectures”,
Krishnan Srinivasan, and Karam S. Chatha,
Proceedings of IEEE International Symposium on Quality Electronic Design (ISQED), March 27-29, San Jose, CA, 2006.

32. “A Technique for Verification of Race Conditions in Real Time Systems”,
Nagendar Telkar, Karam S. Chatha*, Yann-Hang Lee, Gerald Gannod and Eric Wong,
Proceedings of the 2^{nd} *International Workshop on Software Verification and Validation*, Seattle, WA, November, 2004.

33. “ARIA: An Adaptive and Programmable Media-flow Architecture for Interactive Arts”,
Lina Peng, K. Selcuk Candan*, Kyung D. Ryu, Karam S. Chatha and Hari Sundaram,
Proceedings of ACM Multimedia Interactive Art Program (IAP), October 10-15, 2004, New York, NY.

34. “Efficient Stream Routing in Quality- and Resource-Adaptive Flow Architectures”,
K. Selcuk Candan*, **Lina Peng**, Kyung D. Ryu, Karam S. Chatha and Christopher Meyer,
Proceedings of International Workshop on Multimedia Information Systems (MIS), August 25-27, 2004, College Park, MD.

35. “A Technique for Energy versus Quality-of-Service Trade-off for MPEG-2 Decoder”,
Krishnan Srinivasan, and Karam S. Chatha,
Proceedings of IEEE Computer Society Annual Symposium on VLSI, Lafayette, LA, February 19-20, 2004.

36. “An Iterative Algorithm for Partitioning and Scheduling of Area Constrained HW-SW Systems”,
Karam S. Chatha and Ranga Vemuri,
Proceedings of 10th IEEE International Workshop on Rapid Systems Prototyping, Clearwater, Florida, June 16-18, 1999.

37. “Performance Evaluation Tool for Rapid Prototyping of Hardware-Software Codesigns”,
Karam S. Chatha and Ranga Vemuri,
Proceedings of 9th IEEE International Workshop on Rapid Systems Prototyping, Leuven, Belgium, June 3-5, 1998.

38. “Performance Modeling and Tradeoff Analysis During Rapid Prototyping”,
Jeffrey Walrath*, Karam S. Chatha, Ranga Vemuri, Naren Narasimhan and Vinoo Srinivasan,
Proceedings of the 1996 International Conference on Application-Specific Systems, Architectures and Processors, Chicago, IL, August 19-21, 1996.

c. Book Chapter

1. “System-level Design of Network-on-Chip Architectures”,
Karam S. Chatha and **Krishnan Srinivasan**,
Embedded Processor Design - a low power perspective, S. Parameswaran and J. Henkel Eds, Springer Publications, 2007.

Summary of Student Co-Authorship on Publications (in alphabetic order).

- Michael Baker is my current MS student.
- Nilanjan Banerjee was my MS student who graduated in 2004.
- Yinpeng Chen is Prof. Hari Sundaram's PhD student.
- Gisik Kwon is Prof. Selcuk Candan's PhD student.
- Glenn Leary is my current PhD student.
- Jason McCollum was my MS student who graduated in 2005.
- Krishna Mehta was my MS student who graduated in 2007.
- Chris Meyer was Prof. Selcuk Candan's PhD student.
- Chris Ostler is my current MS student.
- Lina Peng is Prof. Selcuk Candan's PhD student.
- Vijay Ramamurthi was my MS student who graduated in 2005.
- Nagendran Rangan was my MS student who graduated in 2003.
- Krishnan Srinivasan was my PhD student who graduated in 2006.
- Nagendar Telkar was my MS student who graduated in 2003.
- Praveen Vellanki was my MS student who graduated in 2004.
- Sushu Zhang is my current PhD student.

d. Invited Presentations

1. System-level Thermal Aware Design,
   IEEE CEDA Distinguished Speaker Series, Cadence Research Labs, Berkeley, CA, May 2008.

2. Design of Communication Infrastructure for System-on-Chip Devices in Nanoscale Technologies,
   Consortium for Embedded Systems, NSF Industry/University Co-operative Research Center (I/UCRC) Planning Meeting, Tempe, AZ, June 2007.

3. System-level Design of Network-on-Chip Architectures,
   Tensilica Inc., Santa Clara, CA, August 2005.

4. Network-on-Chip: Architectures, and Performance Models,
   Xilinx Research Labs, San Jose, CA, June 2004.

5. System-level Cosynthesis of Multimedia Applications,
   Telecommunication Research Center (TRC), Arizona State University, Tempe, AZ, April, 2002.

6. System-level Computer-aided Design Techniques,
   Connection One Kick-off Meeting, Mission Palms Hotel, Tempe, AZ, March 2002.

7. System-level Cosynthesis of Transformative Applications,
   Center for Ubiquitous Computing (CUbiC), Arizona State University, Tempe, AZ, September, 2001.

8. System-level Cosynthesis of Transformative Applications,
   Fujitsu Labs, Sunnyvale, CA, May 2001.

9. System-level Cosynthesis of Transformative Applications,
   Rennselaer Polytechnic Institute, April 2001.

10. System-level Cosynthesis of Transformative Applications,
    Virginia Polytechnic Institute and State University, April 2001.

e. Other Publications

- **"System-Level Cosynthesis of Transformative Applications for Heterogeneous Hardware-Software Architectures"**,
  Karamvir S. Chatha,
  Phd Dissertation, University of Cincinnati, 2001.

- **"Performance Evaluation Tool for Non-pipelined and Pipelined Hardware-Software Codesigns"**,
  Karamvir S. Chatha,
  MS Thesis, University of Cincinnati, 1997.

3 Sponsored Research

Total Awards (8/2001-8/2007): **$ 2,242,668**

Individual share (8/2001-8/2007): **$ 1,041,699** (as lead PI: $ 640,885, as CO-PI: $ 400,814)

Lead PI Federal Grants

No.	*Timeline*	*Title*	*Sponsor*	*Investigators*	*% Recognition /RID/IIA*	*Total Award*	*Individual share*
1	2006-11	CAREER: System-level Design of Network-on-Chip Architectures	NSF	K. S. Chatha	100/100/100	$ 400,000	$ 400,000
2	2006-07	CRI: Collaborative research: Reconfigurable Computing Cluster	NSF	K. S. Chatha, D. Stanzione	50/50/50	$ 14,415	$ 7,207

CO-PI Federal Grants

No.	*Timeline*	*Title*	*Sponsor*	*Investigators*	*% Recognition /RID/IIA*	*Total Award*	*Individual share*
3	2006-08	CNS-SGER: Integrative Security Infrastructure for Personal Identities and Consumer Computing	NSF	P. Dasgupta, K. S. Chatha, S. Gupta	33/33/33	$ 199,890	$ 59,967
4	2005-08	CSR-EHS: Analytical Techniques for Global Energy Minimization of a System of Interacting Components	NSF	C. Chakrabarti, S. Vrudhula, K. S. Chatha	25/25/25	$ 400,000	$ 100,000
5	2003-07	Quality Adaptive Media Flow Architectures to support Sensor Data Management	NSF	S. Candan, K. D. Ryu, K. S. Chatha, H. Sundaram, P. J. Clark	20/20/20	$ 470,000	$ 94,000
6	2002-03	Timing and Race Condition Verification of Real-Time Systems	NASA	Y. H. Lee, G. Gannod, K. S. Chatha, E. Wong	33/33/33	$ 125,164	$ 41,721

Lead PI Industry Grants

No.	*Timeline*	*Title*	*Sponsor*	*Investigators*	*% Recognition /RID/IIA*	*Total Award*	*Individual share*
7	2007-08	Comparative Study and Prototyping of Network-on-Chip in Consumer Electronics ASICs (*$127K, under final stages of IP negotiation with ASU's technology commercialization office (AzTE)*)	Intel Corp.	K. S. Chatha	100/100/100	–	–
8	2004	A Productline Approach for the Development of Network Processor Programming Tools	CES[1]	K. S. Chatha, G. Gannod, R. Govindarajan	50/50/50	$ 90,147	$ 45,073

[3]Consortium for Embedded Systems that has Intel Inc. and Motorola Inc. as members.

Lead PI Industry Grants (continued)

No.	*Timeline*	*Title*	*Sponsor*	*Investigators*	*% Recognition /RID/IIA*	*Total Award*	*Individual share*
9	2004	Graduate-level Course on Hardware/Software Co-design	CES	K. S. Chatha	100/100/100	$ 49,975	$ 49,975
10	2003	Laboratory Development for Capstone Project	CES	K. S. Chatha	100/100/100	$ 84,069	$ 84,069
11	2002-03	Study of Media and Communication Functions on Parallel/Vector Processing Engines for Network Processing Applications	CES	K. S. Chatha, C. Chakrabarti, S. Panchanathan	33/33/33	$ 88,705.	$ 29,568
12	2002-03	Curriculum and Laboratory Development for Advanced Hardware Systems Design	CES	K. S. Chatha, Y. H. Lee	50/50/50	$ 49,987	$ 24,993

CO-PI Industry Grants

No.	*Timeline*	*Title*	*Sponsor*	*Investigators*	*% Recognition /RID/IIA*	*Total Award*	*Individual share*
13	2006	Curriculum development for compiler construction course sequence	CES	R. Bazzi, K. S. Chatha	50/50/50	$ 35,388	$ 17,694
14	2005-06	Integrated Infrastructure for Identity Assurance	CES	P. Dasgupta, K. S. Chatha, S. Gupta	33/33/33	$ 89,789	$ 29,929
15	2005-06	Power Optimization Techniques for a System of Interacting Heterogeneous Components	CES	C. Chakrabarti, S.Vrudhula, K. S. Chatha	33/33/33	$ 90,392	$ 30,130
16	2003	Memory-Efficient Design of Next Generation Communication Processors	CES	C. Chakrabarti, K. S. Chatha	50/50/50	$ 54,747	$ 27,373

4 Student Theses and Dissertations Supervised

a. Doctoral Dissertations Awarded

1. Krishnan Srinivasan — PhD in Computer Science, Arizona State University, 2006.
   Dissertation : Computer-aided design techniques for network-on-chip architectures and system-level low power optimization
   Current position : Sonics Inc.

b. Masters Theses Awarded

1. Krishna Mehta, — MS in Computer Science, Arizona State University, 2007.
   Thesis: Design and implementation of master slave aware network-on-chip architecture on FPGA.
   Current position : Freescale Semiconductor Inc.

2. Nipun Java, — MS in Computer Science, Arizona State University, 2007.
   Thesis: System-level architecture for dynamic partial reconfiguration on FPGAs.
   Current position : St. Jude Medical.

3. Sushobhit Gupt, — MS in Computer Science, Arizona State University, 2006.
   Thesis: Design of router architecture and power/performance models for irregular topology network-on-chip architectures.
   Current position : Cadence Inc.

4. Darshan Kobla, — MS in Computer Science, Arizona State University, 2005.
   Thesis: Design and prototype of NoC based MPSoC architecture on Xilinx FPGA.
   Current position : Intel Corp.

5. Victor Szeto, — MS in Electrical Engineering, Arizona State University, 2005.
   Thesis: Reducing dynamic and leakage power consumption in network-on-chip designs.
   Current position : General Dynamics Inc.

6. Jason McCollum, — MS in Computer Science, Arizona State University, 2005.
   Thesis: Design-time and run-time performance optimization of multiple applications on network processor architectures.
   Current position : Intertel Inc.

7. Vijay Ramamurthi, — MS in Electrical Engineering, Arizona State University, 2005.
   Thesis: A design methodology for mapping applications onto network processors.
   Current position : Motorola Inc.

8. Nilanjan Banerjee, — MS in Electrical Engineering, Arizona State University, 2004.
   Thesis: Quality-of-service and error control schemes for mesh-based network-on-chip architecture.
   Current position : Phd, Purdue University.

9. Praveen Vellanki, — MS in Electrical Engineering, Arizona State University, 2004.
   Thesis: A power and performance model for mesh-based network-on-chip interconnection architectures.
   Current position : Qualcomm Inc.

10. Nagendar Telkar, — MS in Computer Science, Arizona State University, 2003.
    Thesis: Verification of race conditions in real-time systems.
    Current position : Qualcomm Inc.

11. Nagendran Rangan, — MS in Electrical Engineering, Arizona State University, 2003.
    Thesis: A technique for resource-constrained pipelined scheduling during high-level synthesis.
    Current position : Cadence Inc.

c. Current Graduate Students in Progress

1. Michael Baker, PhD (Computer Science), current.
2. Weijia Che, PhD (Computer Science), current.
3. Vinay Hanumiah, PhD (Electrical Engineering), current.
4. Glenn Leary, PhD (Computer Science), current.
5. Sushu Zhang, PhD (Computer Science), current.
6. Parthima Kotikalapudi MS (Computer Science), current.
7. Latha Mukkavilli MS (Computer Science), current.
8. Christopher Ostler, MS (Computer Science), current.

5 Professional and Scientific Service

a. Scientific and Professional Society Memberships

1. Association of Computing Machines (ACM), Special Interest Group on Design Automation (SIGDA), 1998 to present.

2. International Organization of Electrical and Electronic Engineers (IEEE), Circuits and Systems Society, 2001 to present.

b. Conference Activities

1. Finance Chair, IEEE/ACM Symposium on Networks-on-Chip (NOCS), May 2009, San Diego, CA.

2. Finance and Registration Chair, IEEE/ACM Symposium on Networks-on-Chip (NOCS), May 2007, Princeton, NJ.

3. Member of Technical Program Committee

   - IEEE/ACM Design Automation Conference (DAC)
     June 2008, Anaheim, CA; June 2007, San Diego, CA.
   - IEEE/ACM Design Automation and Test in Europe Conference (DATE)
     March 2009, Nice, France; March 2008, Munich, Germany.
   - IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
     November 2008, San Jose, CA.
   - IEEE/ACM Asia South-Pacific Design Automation Conference (ASP-DAC)
     January 2009, Yokohama, Japan; January 2008, Seoul, Korea.
   - IEEE/ACM International Conference on Hardware/Software Co-design and System Synthesis (CODES/ISSS)
     October 2008, Atlanta, Georgia; October 2007, Salzburg, Austria; October 2006, Seoul, Korea.
   - IEEE/ACM Symposium on Network-on-Chip (NOCS),
     April 2008, Newcastle, UK.
   - IEEE International Conference on Application-Specific Systems Architectures and Processors (ASAP)
     July, 2008 Leuven, Belgium; July 2007, Montreal, Canada; September 2006, Steamboat Springs, CO.
   - IFIP International Conference on Embedded and Ubiquitous Computing (EUC)
     December 2007, Taipei, Taiwan.
   - International Conference on Embedded Software and Systems (ICESS)
     May 2007, Daegu, Korea; December 2006, Shanghai, P.R. China.
   - IEEE International SOC Conference (SOCC)
     September 2005, Washington DC.
   - IEEE International Performance Computing and Communications Conference (IPCCC)
     April 2004, Phoenix, AZ.

4. Panel Chair, International Performance, Computing and Communications Conference (IPCCC), April 2003, Phoenix, AZ.

5. Session Chair

   - International Conference on Hardware/Software Co-design and System Synthesis (CODES-ISSS), September 2005, New York Metropolitan Area, NY.
   - International Performance, Computing and Communications Conference (IPCCC), April 2002, Phoenix, AZ.

c. Journal Referee Service

1. Guest Editor, *Special Issue: Circuits and Systems for Real-Time Security and Copyright Protection of Multimedia*, International Journal of Computers and Electrical Engineering, Elsevier Publications, December 2007/January 2008.
2. Manuscript reviewer for
    - ACM Transactions on Design Automation for Electronic Systems
    - ACM Transactions on Embedded Systems
    - IEEE Transactions on Computer-Aided Design of Integrated Circuits
    - IEEE Transactions on VLSI Systems
    - IEEE Transactions on Computers
    - IEEE Transactions on Signal Processing
    - IEEE Micro
    - Elsevier Journal of Systems Architecture

d. Proposal Referee Service

1. Expert of international standing on Australian Research Council for assessing grant proposals in 2007, 2006, and 2005.

e. Ira A Fulton School of Engineering Service

1. Chair, Research Committee, Consortium for Embedded Systems, October 2002 - May 2004.
2. Organized ”Consortium for Embedded Systems: New Initiatives Workshop”, November 14th, 2005.

f. Department of Computer Science and Engineering Service

1. Chair, CSE Undergraduate Curriculum Committee, 2006-2007.
2. Systems Area, Technical Area Committee, 2001-present.
3. CSE Undergraduate Curriculum Committee, 2007-2008.
4. CSE Graduate Admissions Committee, 2005-2007.
5. CSE Faculty Recruiting Committee, 2002-2004.
6. CSE Computing Resources Committee, 2002-2003.
7. CSE Graduate Admissions Committee, 2001-2002.

6 Evaluation of Instruction

a. Summary of student evaluations[4]

No.	Semester	Course	Title	Class size	Score (out of 5)
1.	Spring 08	CSE 494/598	System-level Hardware-Software Co-design	39	4.7
2.	Spring 08	CSE 424	Systems Capstone Project II	18	4.46
3.	Fall 07	CSE 320	Design and Synthesis of Digital Hardware	50	4.61
4.	Spring 07	CSE 494/598	System-level Hardware-Software Co-design	13	4.95
5.	Fall 06	CSE 320	Design and Synthesis of Digital Hardware	55	4.68
6.	Fall 06	CSE 591	System-level Hardware-Software Co-design	39	3.64[5]
7.	Spring 06	CSE 422	Micro-computer System Design	52	4.51
8.	Fall 05	CSE 422	Micro-computer System Design	44	4.55
9.	Fall 05	CSE 591	Hardware-Software Co-design	10	3.9[6]
10.	Fall 05	CSE 591	Advance Hardware Systems Design (Online course)	9	3.81[7]
11.	Spring 05	CSE 591	Hardware-Software Co-design	8	4.4
12.	Fall 04	CSE 494/598	Electronic Design Automation	9	3.95
13.	Fall 04	CSE 422	Micro-computer System Design	41	4.36
14.	Spring 04	CSE 494/598	Electronic Design Automation	11	4.69
15.	Spring 04	CSE 423	Micro-computer System Hardware	47	4.06[8]
16.	Fall 03	CSE/EEE 517	Hardware Design Language	43	4.13
17.	Spring 03	CSE 423	Micro-computer System Hardware	33	4.15
18.	Fall 02	CSE/EEE 517	Hardware Design Language	58	4.06
19.	Spring 02	CSE 591	Hardware-Software Co-design	31	4.64
20.	Fall 01	CSE/EEE 517	Hardware Design Language	117	4.24

b. Curriculum and laboratory development

1. CSE 320: Design and synthesis of digital hardware
2. CSE 423: Systems Capstone Project I
3. CSE 494/598: Electronic design automation
4. CSE 494/598: System-level hardware-software co-design

c. Undergraduate Projects Supervised

1. Stephanie Handrick, Individualized instruction, CSE 499, "Study of IP look-up Algorithms", Spring 2007.
2. Logan J. Hall, Supreet Nagi, Jon Sargeant and Sirish Shetty, Capstone project, CSE 423, "HW versus SW trade-off for AES Encryption/Decryption Algorithms", Spring 2004.
3. Ismar Alikadic, Haissam Hamze, Ahmet Kurdoglu, Ahmet Ince and Tzu-Hsin Lu, Capstone project, CSE 423, "HW versus SW trade-off for DCT and FFT signal processing algorithms", Spring 2004.
4. Christopher Ostler, Joseph Vahabzadeh, Andrew Suft, Keith Wallace and Christopher Bertrand, Capstone project, CSE 423, "HW versus SW trade-off for IP look-up and VLD Algorithms", Spring 2004.
5. Michael Fanning, Hoshil Desai and Rami Mostofo, Capstone project, CSE 423, "HW versus SW trade-off for AES Encryption/Decryption Algorithms", Spring 2003.
6. Stephen Bent, Daniel Butters, David Watkins and Benjamin Moore, Capstone project, CSE 423, "HW versus SW trade-off for DCT and FFT signal processing algorithsm", Spring 2003.
7. James Oranski, Mathew Cicalese and Dennise Castrillon, Capstone project, CSE 423, "HW versus SW trade-off for IP look-up and VLD Algorithms", Spring 2003.
8. Ziyad Saeed, Individualized instruction, EEE 498, "Evaluation of Xilinx FPGA for Sensor Networks", Fall 2003.

[4] Average score has been presented for courses with multiple sections.

[5] New textbook, laboratory set-up and new semester long project.

[6] New topics and new semester long project.

[7] "Advanced Hardware Systems Design" was a new course exclusively offered online through Center of Professional Development (CPD) as part of the Executive Embedded Systems degree program. This was the first time that I was offering a course that was solely delivered through the web.

[8] CSE 423 is the capstone project for BS(CSE) program. Groups of students work with individual advisors (other than the instructor) on their projects. Thus, the evaluation score includes feedback about the project advisor and the instructor.